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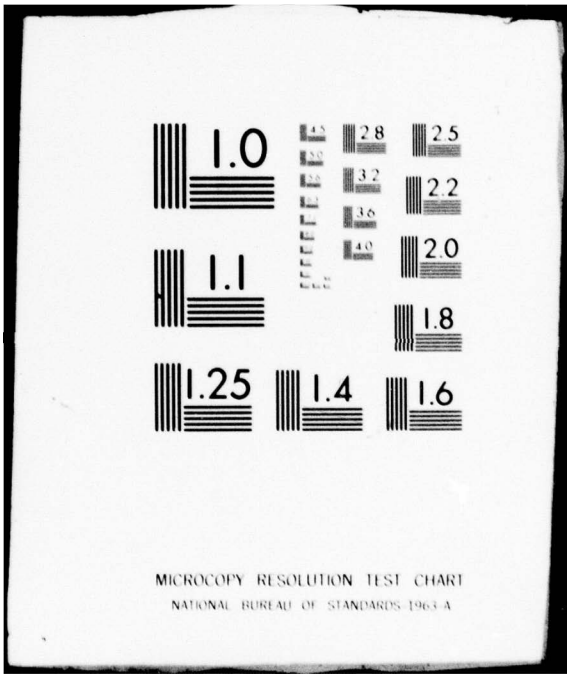
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SURFACE AND INTERFACE DEPLETION CORRECTIONS TO FREE CARRIER DENSITY DETERMINATIONS BY HALL MEASUREMENTS

by

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ABSTRACT

Errors in the determination of $(N_D - N_A)$ for semiconductor epitaxial layers by the Hall method can result if corrections for carrier depletion are omitted in the calculations. Simple practical procedures are discussed to correct for carrier depletion that occurs in epitaxial layers at their free surfaces, and their interfaces with semi-insulating substrates. Theoretical estimates of carrier depletion in GaAs indicate that depletion regions can extend several microns into high purity epitaxial layers, and can cause $(N_D - N_A)$ to be considerably underestimated. Experimental evidence is presented in support of the theory.

I. INTRODUCTION

Characterization of semiconductor epitaxial layers usually includes the determination of free carrier density $(N_D-N_A)^*$ by Hall measurement and C-V profiling. This paper draws attention to errors which can be made in interpreting the data from the former method if depletion effects caused by surface state pinning of the Fermi level and the band bending at the interface with semi-insulating substrates are not considered. For uniform samples, Hall measurements essentially determine the free carrier density per unit area, Q, given by

$$Q = \frac{r_H \, I \, B}{q \, V_H} \qquad (1)$$

where r_H is the Hall scattering factor, I the current, B the magnetic field normal to the current, V_H the Hall voltage normal to both I and B, and q the electronic charge.

The free carrier density per unit volume, n, can be obtained from Q by the equation

$$n = \frac{Q}{\ell_e} , \qquad (2)$$

where ℓ_e is the thickness of the region that is electrically

*Strictly speaking the free carrier density can be significantly less than N_D-N_A at low temperatures and higher carrier densities ($> 10^{15}$), however in most cases at room temperature the ionization is close to 100%.

conducting. This may not be the same as the metallurgical thickness of the epilayer, ℓ_m.

II. FREE SURFACE DEPLETION

In fact, if surface states pin the Fermi level at the surface to a value E_{FS} in the forbidden gap, (as is usually the case for air exposed or chemically prepared semiconductor surfaces), then carrier depletion occurs in the region below the surface. Depleted carriers become trapped in immobile surface states and do not contribute to the electrical conductivity and hence the Hall voltage [1].

The built-in potential V_{BS} is given by

$$V_{BS} = \phi_B - \frac{kT}{q} \ln \frac{N_c}{N_D - N_A} \tag{3}$$

where $\phi_B = E_{CS} - E_{FS}$, k is the Boltzmann constant, T is the temperature, N_c is the effective density of states at the conduction band minimum, and E_{FS} and E_{CS} are the Fermi level and the conduction band minimum respectively at the surface (Fig. 1). N_c is obtained from [2].

$$N_c = 4.83 \times 10^{15} \times (m_n^*/m_o)^{3/2} \; T^{3/2} \; cm^{-3}$$

where (m_n^*/m_o) is the relative density of states effective

mass of electrons.

In the abrupt depletion edge approximation, this leads to a depletion width at the surface given by

$$\left[\frac{2\varepsilon\varepsilon_o V_{BS}}{q(N_D-N_A)}\right]^{1/2}$$

where ε_o is the permittivity of free space, and ε is the relative permittivity of the semiconductor. More accurately, the effective depletion width ℓ_s, defined as the ratio of the charge depleted per unit area to N_D-N_A is obtained by [3].

$$\ell_s = \left[\frac{2\varepsilon\varepsilon_o(V_{BS} - kT/q)}{q(N_D-N_A)}\right]^{1/2} \qquad (4)$$

Using equations (3) and (4), if ϕ_B is known, then ℓ_s can be calculated as a function of (N_D-N_A).

In the specific case of GaAs, it has been found from $1/C^2$ vs. V extrapolations for Schottky barriers evaporated in-situ onto M.B.E. films that the Fermi level is pinned in all normal surfaces at approximately 0.6 eV below the conduction band. [4] Photoemission measurements agree with this value. [5]

Higher values determined by metal Schottky barrier I-V and C^{-2}-V extrapolations have been shown [6] to be caused

by interfacial oxides, and as such do not contribute to the surface region depletion. Thus the lowest measured value of the surface barrier height should be used in the corrective procuedure suggested herein.

Fig. 2(a) shows the surface depletion width ℓ_s calculated for GaAs using ϕ_B = 0.6 eV, plotted against N_D-N_A.

III. INTERFACE DEPLETION

Carrier depletion from the layer at its interface with the S.I. substrate depends on the density of free carriers (N_D-N_A) in the epilayer relative to the density of unfilled electron traps N_T in the substrate. (These traps could be unionized deep acceptors, such as chromium, or ionized deep donors, such as oxygen).

Electrons diffuse from the n region to the substrate and become trapped in the unfilled deep levels, where they are immobilized. The space charge region on the semi-insulating side has a negative density N_T. The contact potential, given by

$$V_{BI} = \frac{(E_C - E_T)_{S.I.}}{q} - \frac{kT}{q} \ln \frac{N_c}{N_D-N_A} \qquad (5)$$

(where E_T is the energy level of the electron traps) is divided into components V_n and V_{SI} equal to the band bending on the n and the S.I. sides of the interface respectively (Fig. 3(a)).

Assuming, for simplicity, the abrupt space charge region approximation, V_n is obtained from the equations

$$V_n + V_{SI} = V_{BI}$$

$$V_n/V_{SI} = N_T/(N_D-N_A)$$

so that

$$V_n = V_{BI}\left[1 + \frac{N_D-N_A}{N_T}\right]^{-1}, \qquad (6)$$

which leads to a general expression for the interface depletion width

$$\ell_i = \left[\frac{2\varepsilon\varepsilon_o(V_n - kT/q)}{q(N_D-N_A)}\right]^{1/2} \qquad (7)$$

in analogy with Eq. (4).

The density N_T varies widely for commercially available semi-insulating GaAs, typically in the range 10^{15} to 10^{17} cm^{-3} and its value is not usually available, or easily determined. This restricts the usefulness of equations (6) and (7). However, for low doped n^- layers (FET buffer layers, for example) with n in the 10^{13} or 10^{14} cm^{-3} range, N_D-N_A can be assumed $<< N_T$, so then $V_n \simeq V_{BI}$ (Fig. 3(b)) and

$$\ell_i = \left[\frac{2\varepsilon\varepsilon_o(V_{BI} - kT/q)}{q(N_D-N_A)}\right]^{1/2} \qquad (8)$$

The chromium trap level in GaAs has been measured to be approximately 0.75 eV below E_C [7,8]. Using this value, ℓ_i is plotted against (N_D-N_A) in Fig. 2(b).

At the other extreme, if (N_D-N_A) is >> N_T, as can be the case for FET active layers grown directly on S.I. substrates, partial depletion occurs in the epilayer to a depth of the order of λ_D, where

$$\lambda_D = \left[\frac{\varepsilon\varepsilon_o kT}{q^2(N_D-N_A)}\right]^{1/2}$$

is the debye length of the n layer. For $N_D-N_A = 10^{17}$ cm^{-3} in GaAs, λ_D at 300°K is ≃ 140 Å, so ℓ_i can usually be neglected. Furthermore, the space charge created in the substrate by electrons diffusing in from the epilayer, consists largely of free carriers (Fig. 3(c)) within a few debye lengths from the interface. This further reduces the effective interface depletion width.

The electrical thickness of the epilayer should hence be taken as $\ell_e = \ell_m-\ell_s-\ell_i$ to account for surface and interface depletion.

Of course, for homogeneous Hall samples, the correction would be $\ell_e = \ell_m - 2\ell_s$.

IV. PRACTICAL APPLICATIONS

1) <u>High purity GaAs "buffer layers"</u>:

It is seen from Fig. 2 that for high purity material,

the total depletion thickness can be several microns. To achieve high purity epitaxial layers by LPE, it becomes necessary to grow at low temperatures ($\approx 700^{\circ}C$) [9]. This significantly limits the thickness of epilayers that can be grown conveniently (to about 15 microns). In such situations, the thickness correction factor ℓ_m/ℓ_e for N_D-N_A can be considerable. Indeed, if $\ell_s + \ell_i$ exceeds ℓ_m, the entire layer will be depleted, and no conduction will be observed in the absence of light.

2) GaAs FET Layers:

Another practical situation that requires correction for depletion, is the characterization of submicron GaAs FET active layers doped at $\approx 10^{17}$ cm^{-3} grown on semi-insulating substrates with or without a high sheet resistivity buffer layer. In Fig. 4, calculated values of the apparent (N_D-N_A) are plotted against the real (N_D-N_A) assuming $\ell_e = \ell_m - \ell_s$.

3) Surface Conversion:

A third practical case to be considered is that of surface electrical conversion of semi-insulating substrates on heat treatment [10]. When quantitative estimation of the free carrier density formed by conversion is carried out by sheet conductivity or Hall measurements, e.g. [11], the surface and interfacial depletion corrections will re-

sult in an underestimation of the extent of conversion or indicate no conversion at all.

Finally, if a layer is grown on such a semi-insulating substrate with a p^+ converted surface, not only does the p^+ layer cause a depletion width given by Eq. (8), with

$$V_{BI} \simeq \frac{1}{q} \left\{ E_g - kT \ell_n \frac{N_c}{N_D - N_A} \right\}$$

but it can also conduct in parallel with the epilayer*, causing the measured value of the electron mobility in the layer, μ_n', to be low. For such a case a simple analysis shows that

$$\mu_n' = \frac{\sigma_{\square n}\mu_n - \sigma_{\square p}\mu_p}{\sigma_{\square n} + \sigma_{\square p}} \qquad (9)$$

where

$\sigma_{\square n} = qnt_n\mu_n$ is the sheet conductivity of the n layer.

$\sigma_{\square p} = qpt_p\mu_p$ is the sheet conductivity of the p^+ conversion layer.

t_n and t_p are the electrical thicknesses of the n and the p^+ layers, and

*This will happen when the tin dots used for alloyed ohmic contacts to the epilayer also form $n^+ - p^+$ junctions with the underlying p^+ conversion region, and when the voltages that develop across the contacts cause these junctions to break down.

μ_n and μ_p are the majority carrier mobilities in the two regions.

Usually $\sigma_{\square n}\mu_n >> \sigma_{\square p}\mu_p$, which gives

$$\mu_n' \simeq \mu_n (1 + \sigma_{\square p}/\sigma_{\square n}). \quad (10)$$

This discussion has treated only n type material. However, p-type material is subject to an analogous treatment. Fermi level pinning by surface states causes band bending in the opposite direction, and a depletion region exists at the surface. An analogous treatment is also valid at the interface with a semi-insulating substrate, where the density of excess electron traps, N_T, is replaced by the density of occupied deep levels.

V. EXPERIMENTAL RESULTS

As an example of the application of the foregoing concepts, Figure 5 shows the results of a Hall study of Sn doping in 16 epilayers of varying thickness listed in Table I, grown on semi-insulating substrates by liquid phase epitaxy. The magnetic field for the measurements was 2 KG., and the sample type was a 6 point "bridge" ultrasonically cut through the epilayer with the substrate remaining to support the layer and its contact arms. The lower line in Fig. 5 is a least squares fit to the uncorrected net carrier concentration calculated from Equations (1) and (2), with the values of r_H obtained

from theoretical calculations to be published by A. Chandra.[12] The upper line is a least squares fit to the points after they have been adjusted for surface and interface depletion widths found from Figs. (2a) and (2b), respectively, using an interative procedure. Also indicated by the circled points are values of N_D-N_A obtained from Schottky barrier capacitance measurements on 3 epilayers with Sn doped n^+ substrates, grown simultaneously with 3 of the Hall samples. It can be seen that the depletion corrections have produced agreement between Hall and capacitance measurements within 12% which is just within the experimental errors for the two methods. Without the correction there is a 30% discrepancy at $1x10^{15}/cm^3$, and even larger percentage discrepancies at lower doping.

Possible differences in carrier concentration in epilayers on the two types of substrate due, for example, to diffusion from the substrate, have been discounted on the basis of the following: (1) The doping profile of layers on the n^+ substrates is flat to within a few percent over 90% of the thickness; (2) Capacitance measurements made on other epilayers on semi-insulating substrates are in agreement with these results as long as the undepleted portion of the layer is thick enough to avoid contribution of a significant series resistive component to the diode impedance; (3) Properties of the layers are unaffected by differences in growth time; (4) Analysis of 77^oK mobility indicates on the order of only

$1.5 \times 10^{14}/cm^3$ residual ionized impurities, and (5) The results are in agreement with other measurements of the Sn distribution coefficient made on layers with higher doping times thickness product.[13]

V. ACKNOWLEDGEMENTS

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David Woodard - Air Force Office of Scientific Research.

Table II-1. Properties of Epilayers at 77°K

Wafer No.	Thickness, ℓm (μm)	[Sn] at %	Hall factor, r_H	$\frac{r_H IB}{eV_H \ell m}$ $\times 10^{14}/cm^3$	$\frac{r_H IB}{eV_H[\ell_m-(\ell_s+\ell_i)]}$ $\times 10^{14}/cm^3$
3652-12-130	21.1	.0069	1.15	0.973	1.30
3652-12-132	18.0	.0069	1.15	0.584	.898
SI-637	5.0	.0072	1.21	0.269	1.96
3652-104A	5.4	.010	1.23	0.938	2.80
3652-104B	5.5	.010	1.18	1.28	3.23
3652-105A	8.1	.010	1.22	1.33	2.50
SI-638	6.8	.0145	1.24	1.63	3.22
3652-2-126	10.4	.0199	1.20	3.39	4.63
SI-639	5.0	.0215	1.23	3.07	6.37
SI-643	6.4	.0237	1.28	4.22	6.91
SI-644	5.1	.0237	1.26	3.28	6.64
SI-640	3.7	.0286	1.26	3.96	8.77
SI-641	4.4	.0358	1.26	5.50	9.83
3652-106A	8.7	.040	1.29	8.39	10.64
3652-109	5.0	.040	1.29	6.34	10.17
SI-642	3.7	.082	1.37	16.3	24.22

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VII. FIGURE CAPTIONS

Fig. 1 Simplified model of surface band bending associated with surface state pinning of the Fermi level.

Fig. 2 The estimated (a) surface depletion width ℓ_s and (b) interface depletion width ℓ_i, as functions of free carrier densities in n:GaAs at 77°K and 295°K.

Fig. 3 Simplified band diagrams at the n epilayer - S.I. substrate interface for

(a) $N_D - N_A \simeq N_T$

(b) $N_D - N_A << N_T$

and (c) $N_D - N_A >> N_T$

where N_T = excess trap density in the substrate.

Fig. 4 Calculated curves for apparent net donor density vs. real net donor density in GaAs at room temperature, for $N_D - N_A >> N_T$, assuming $\phi_B = 0.6V$, for various epilayer thicknesses ℓ_m. (For $(N_D - N_A) >> N_T$ interface depletion is unimportant).

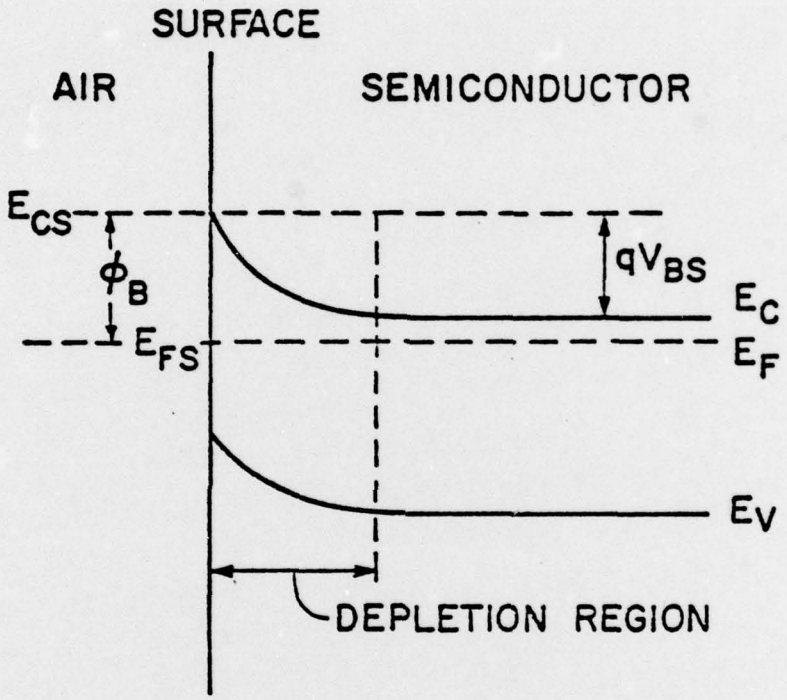
Fig. 5 $N_D - N_A$ as a function of Sn concentration in the melt for the epilayers listed in Table I.

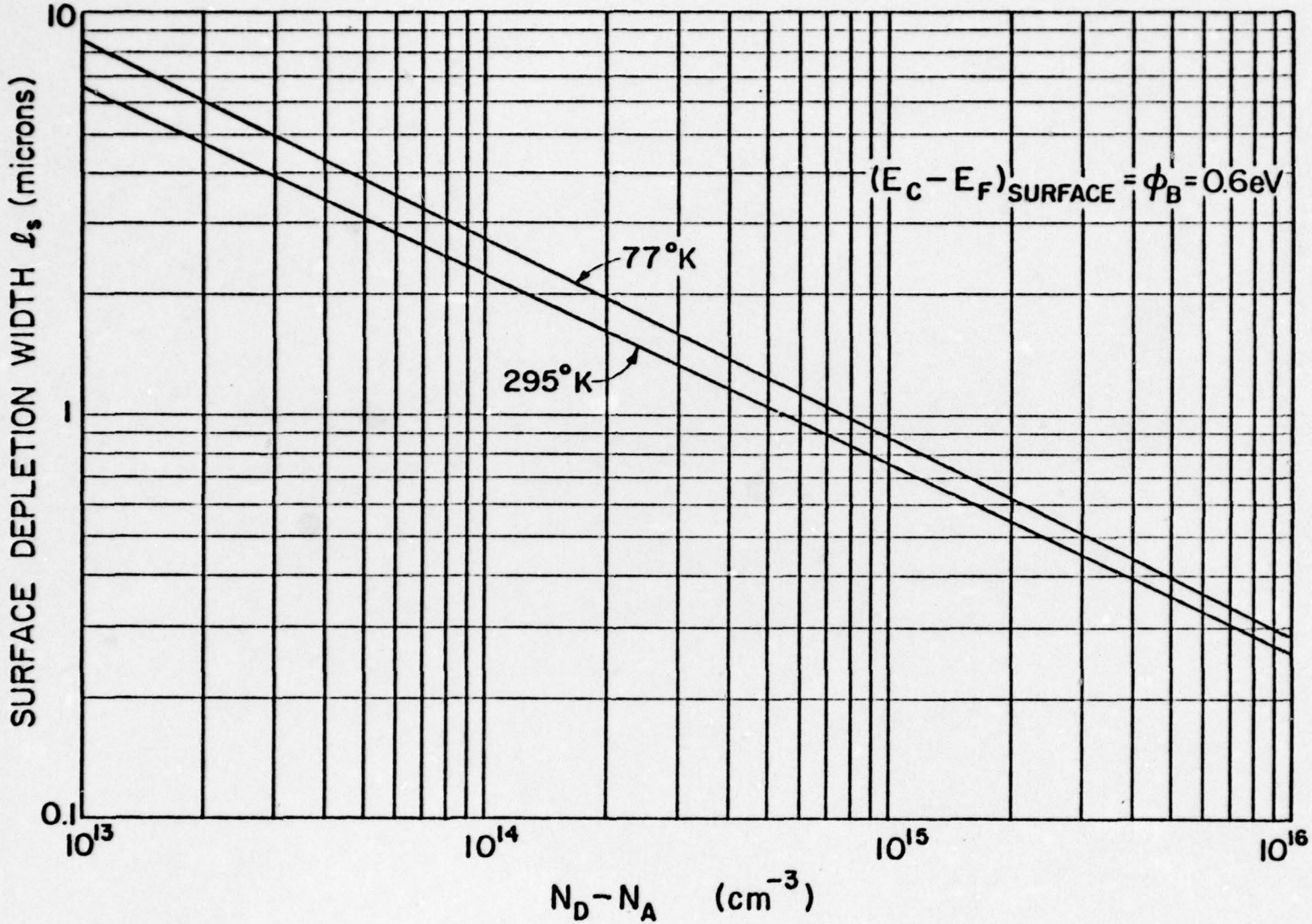
LIST OF SYMBOLS

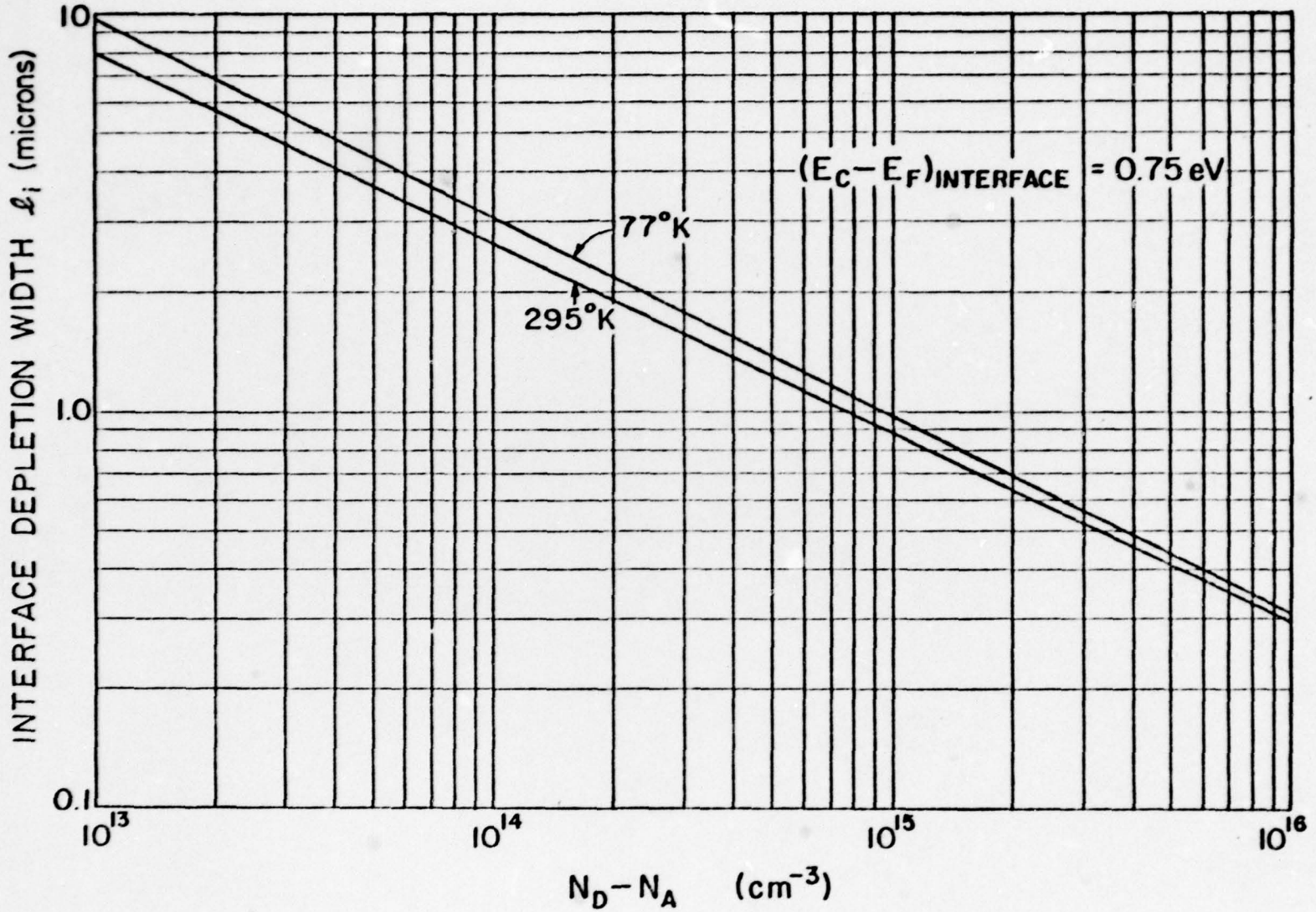
N_D-N_A	net donor density (assumed equal to the free electron concentration), $meter^{-3}$.
Q	free carrier density per unit area, $meter^{-2}$.
V_H	Hall factor, dimensionless.
I	Current, amperes.
B	Magnetic field, $Webers/meter^2$.
q	Electronic charge, coulomb.
V_H	Hall voltage, volts.
n	Free electron density.
ℓ_e	electrical thickness of epilayer, meters.
ℓ_m	metallurgical thickness of epilayer, meters.
ℓ_s	effective surface depletion thickness, meters.
ℓ_i	effective interface depletion thickness, meters.
V_{BS}	Built in potential at surface, volts.
ϕ_B	Surface barrier height, volts.
k	Boltzman constant, eV/Kelvin
T	Temperature, ^oKelvin
N_c	Effective density of states at conduction band edge, cm^{-3}.
E_{FS}	Fermi level at surface, eV.
E_{CS}	Conduction band minimum at surface, eV.
m_n^*	Effective mass (density of states) of electrons, gm.
m_o	Real electron mass, gm.
ε	Dielectric constant (static).
ε_o	Permitivitty of free space farads/meter.

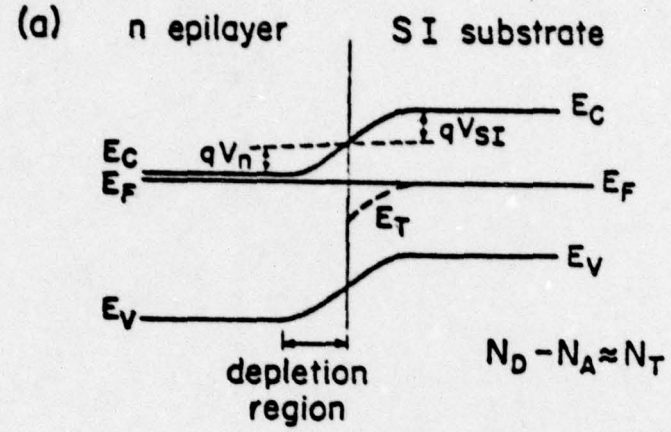
N_T	Density of unfilled electron traps.
V_{BI}	Built in potential at interface.
E_c	Conduction band mimimum, eV.
E_T	Trap level, eV.
V_n	Band bending at interface on n side.
V_{SI}	Band bending at interface on SI side.
λ_D	Debye length in epilayer, meters.
Eg	Band gap, eV.
μ_n'	Measured electron mobility of n epilayer grown on p^+ conversion layer, $cm^2/V.sec$.
μ_p	Hole mobility in p^+ converted layer.
$\sigma_{\square n}$	Sheet conductivity of n epilayer, mhos.
$\sigma_{\square p}$	Sheet conductivity of p^+ converted layer, mhos.
t_n	Electrical thickness of n epilayer, cm.
t_p	Electrical thickness of p^+ layer, cm.

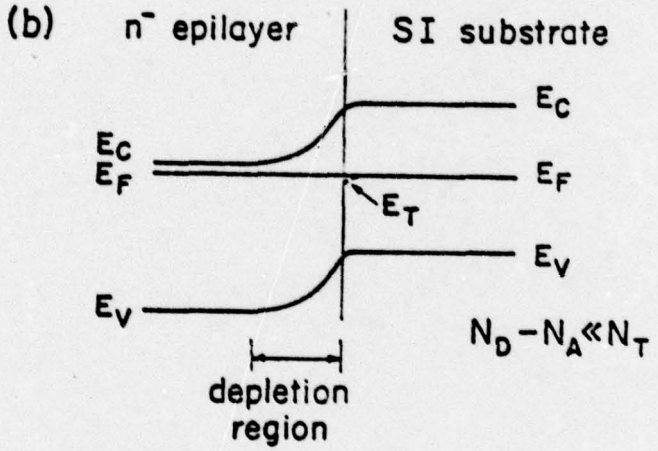
Note: In all equations, mksc units are used unless specifically mentioned otherwise. However, after calculations, several of the quantities may be converted to practical units, and quoted thus.

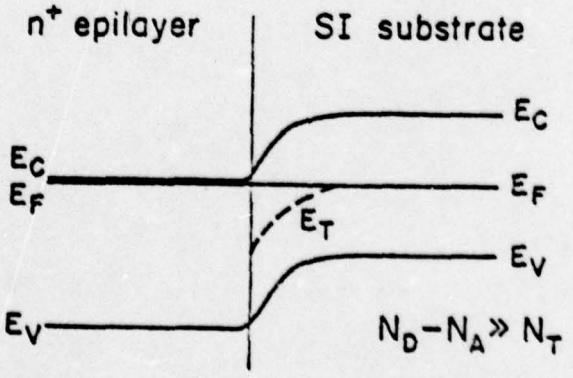

SURFACE
AIR
SEMICONDUCTOR
E_{CS}
ϕ_B
E_{FS}
qV_{BS}
E_C
E_F
E_V
DEPLETION REGION

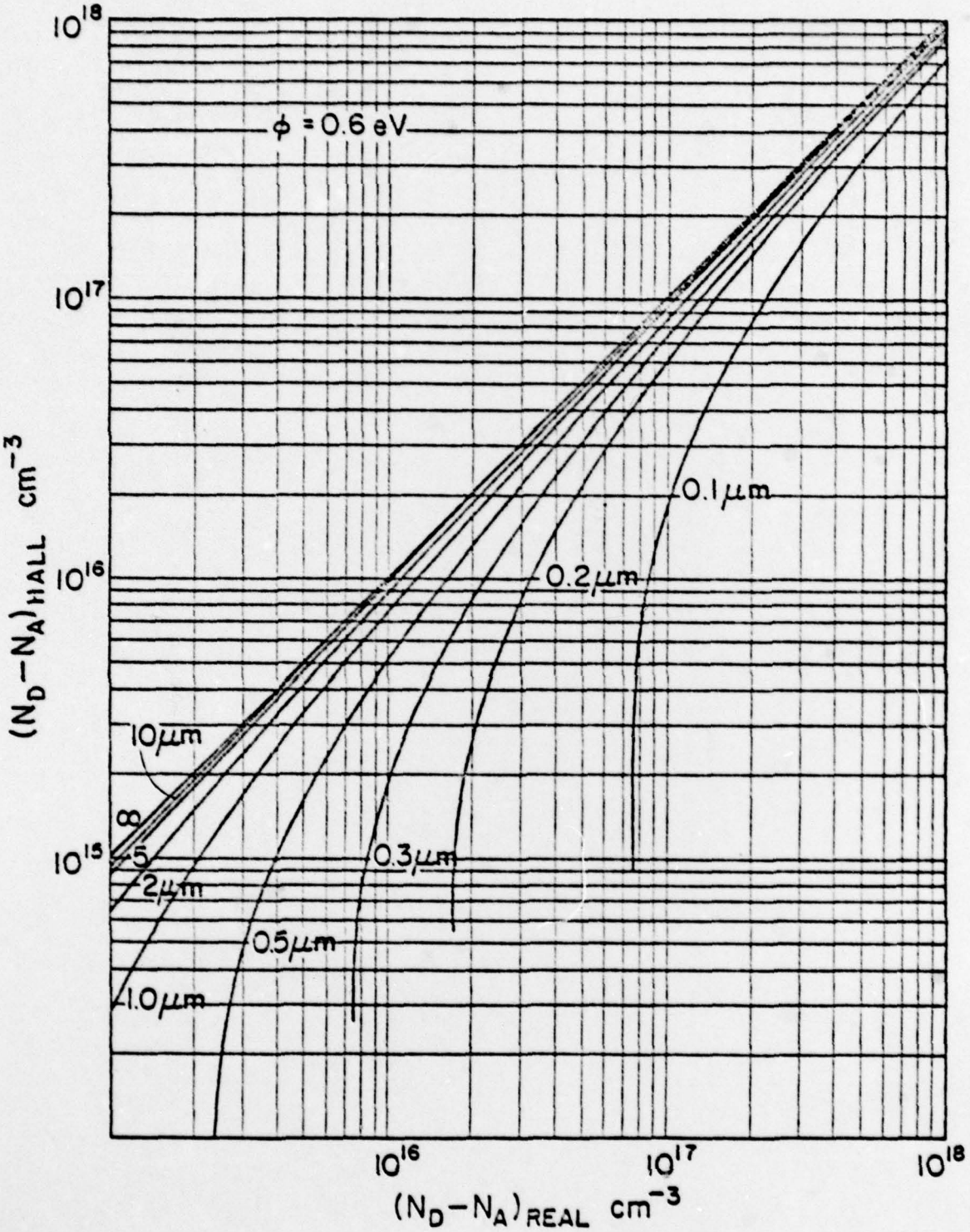

10
1
0.1
SURFACE DEPLETION WIDTH ℓ_s (microns)
$(E_C - E_F)_{SURFACE} = \phi_B = 0.6eV$
77°K
295°K
10^{13}
10^{14}
10^{15}
10^{16}
$N_D - N_A$ (cm^{-3})

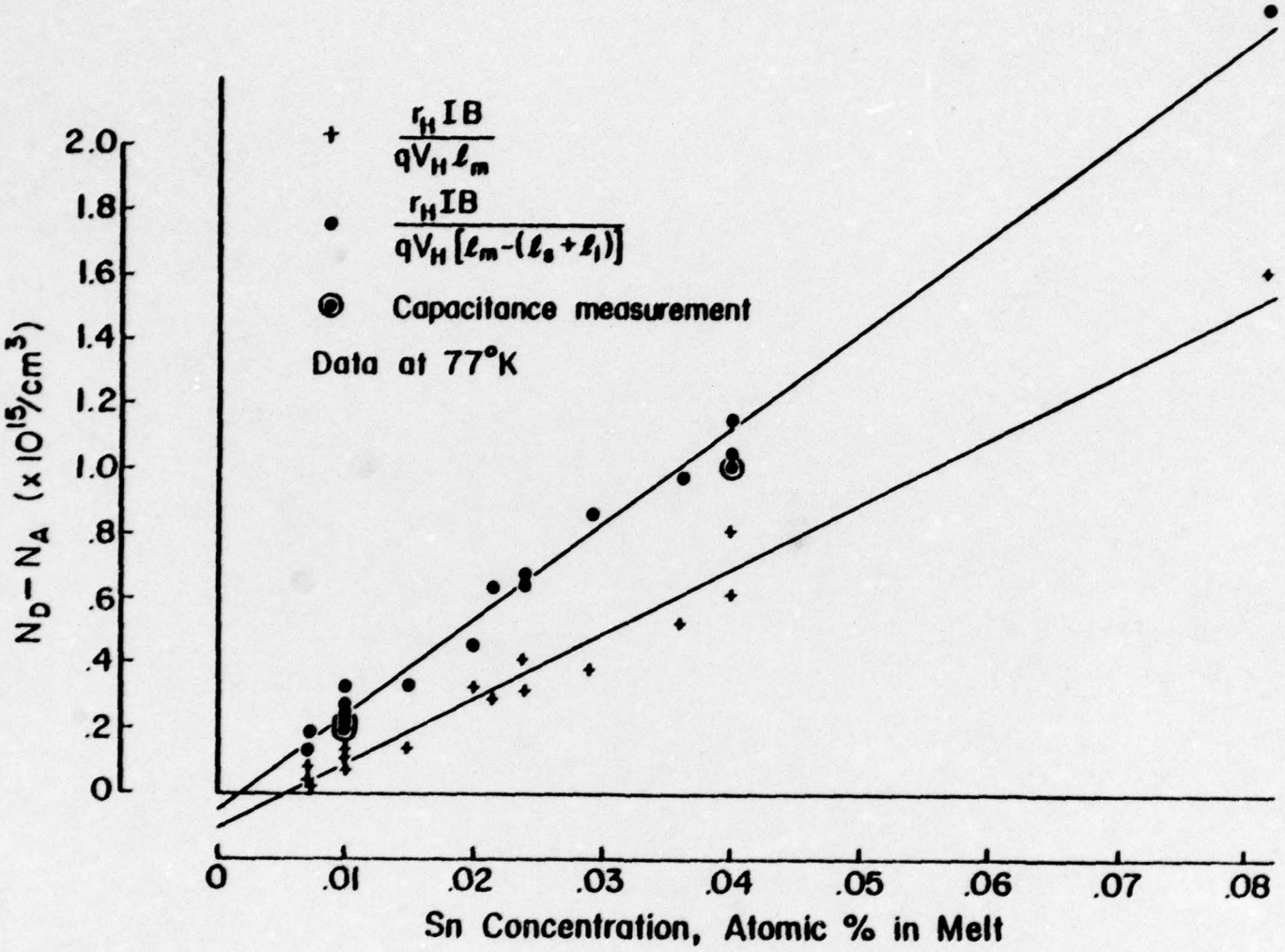

10
1.0
0.1
INTERFACE DEPLETION WIDTH ℓ_i (microns)
$(E_C - E_F)_{INTERFACE}$ = 0.75 eV
77°K
295°K
10^{13}
10^{14}
10^{15}
10^{16}
$N_D - N_A$ (cm^{-3})


(a)
n epilayer
SI substrate
E_C
qV_{SI}
E_C
qV_n
E_F
E_F
E_T
E_V
E_V
$N_D - N_A \approx N_T$
depletion region


(b)
n^- epilayer
SI substrate
E_C
E_C
E_F
E_F
E_T
E_V
E_V
$N_D - N_A \ll N_T$
depletion region


(c)
n^+ epilayer
SI substrate
E_C
E_C
E_F
E_F
E_T
E_V
E_V
$N_D - N_A \gg N_T$


10^{18}
10^{17}
10^{16}
10^{15}
$\phi = 0.6$ eV
0.1 μm
0.2 μm
0.3 μm
0.5 μm
1.0 μm
2 μm
5
8
10 μm
$(N_D - N_A)_{HALL}$ cm^{-3}
10^{16}
10^{17}
10^{18}
$(N_D - N_A)_{REAL}$ cm^{-3}


$\frac{r_H IB}{qV_H \ell_m}$
$\frac{r_H IB}{qV_H [\ell_m - (\ell_o + \ell_i)]}$
Capacitance measurement
Data at 77°K
$N_D - N_A$ (x 10^{15}/cm^3)
2.0
1.8
1.6
1.4
1.2
1.0
.8
.6
.4
.2
0
0
.01
.02
.03
.04
.05
.06
.07
.08
Sn Concentration, Atomic % in Melt